Delcom USB Low Speed IO Chip Migration Document.
802x00 (Cypress CYC7C63x01) Discontinued Part
802x70 (Cypress CYC7C637x3) Replacement Part
June 29, 2005 – Rev 1 - Preliminary

Summary:
This document describes the migration from the Delcom USB Low Speed IO Chip 802x00 (Cypress PN CY7C63x01) to the Delcom USB Low Speed IO Chip 802x70 (Cypress PN CY7C637x3). Cypress semiconductor (the chip manufacture) has discounted the CY7C63x01 family because of RoHS compliance. Cypress has introduced the CY7C637x3 family, which will be RoHS compliant.

Should you upgrade?
We will continue to supply the older chips for as long as we can get them. But eventually stock will decline. Also the RoHS mandate is approaching, and your end product should meet these requirements.

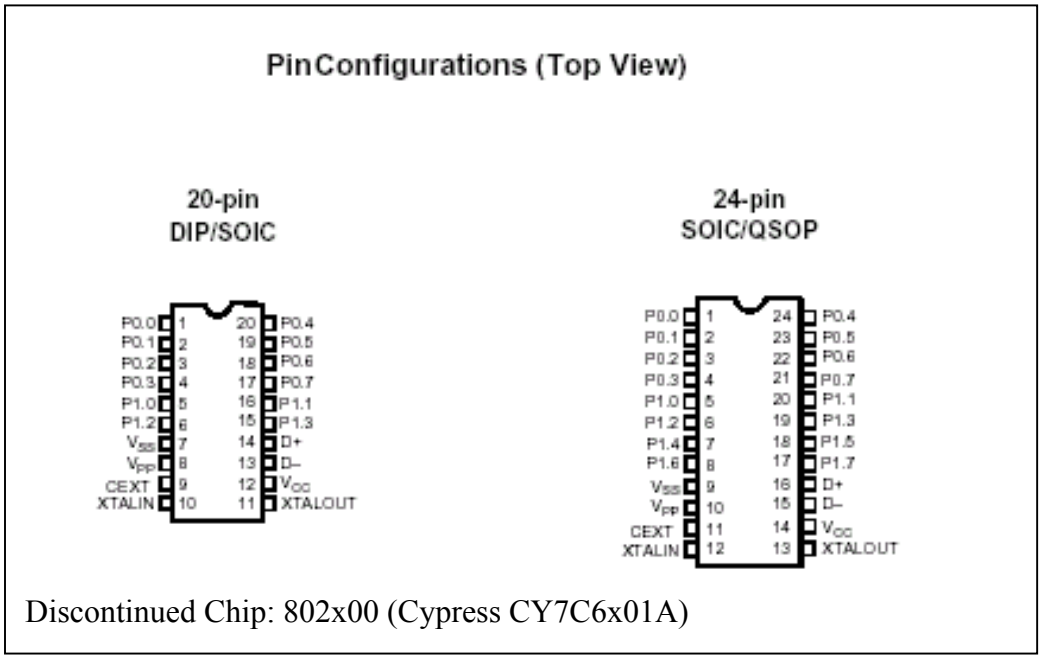
Compatibility:
We have tried to make the migration as simply as possible and have made the chips as backwards compatible as possible. For most applications the new chip should be a drop in replacement. However there are two major hardware differences; the new chips have different port structures and the SOIC/DIP 20 package long longer exists. From a software stand point there are only minor differences(see below). The same Delcom USB driver and command structure is used.

Crossover Table:

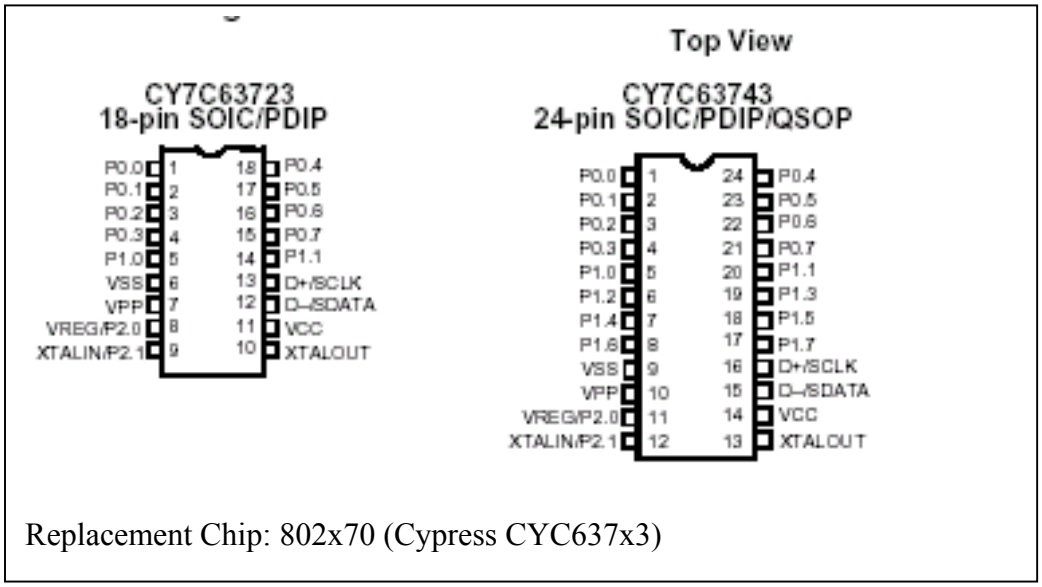
Discontinued Part	**Replacement Part**	
802200 – SOIC20 (Cypress CYC7C6001A-SC)	802270 – SOIC18 (Cypress CYC7C6723-SC)	
802300 – DIP20 (Cypress CYC7C6001A-PC)	802370 – DIP18 (Cypress CYC7C6723-PC)	
802600 – SOIC24 (Cypress CYC7C6101A-SC)	802670 – SOIC24 (Cypress CYC7C6743-SC)	
	802770 – DIP (Cypress CYC7C6743-PC)	

Package Differences:
The new chips are available in SOIC/DIP18 and SOIC/DIP24. For users currently using the SOIC24 package the new SOIC24 chip will be a direct replacement. Users currently using the SOIC/DIP20 packages will have to choose between the SOIC/DIP18 or SOIC/DIP24 packages. See package pin out diagram below.

For SOIC/DIP20 users it maybe possible to mount a SOIC/DIP18 or SOIC/DIP24 package on a SOIC/DIP20 PCB layout. This is possible because the bottom of the chip has the same pin out. Leaving the user to only reconfigure the IO pins via software. For those of you using the fixed pin functions (eg RS232 or I2C), contact us to have the fixed pin functions moved.



Discontinued Chip: 802x00 (Cypress CY7C6x01A)



Replacement Chip: 802x70 (Cypress CYC637x3)

Port Structures Differences:
The old chip IO port pin structure consisted of an open drain with a 16K-ohm pull up resistor. The IO port sink current was configurable and the pull up resistor could be disabled. The default boot up state was a high level with 16K pull up enabled and maximum sink current.
Old commands to change the sink current and pull up are now ignored. See commands 10-30, 10-31, 10-32 and 10-33.

The new chip IO port pins can be set in one of four different modes. Each pin can be changed independently. See IO Port Mode below. The default boot up state is mode 2, which is similar to the old chip. High level with 14K pull up enabled and 2mA sink current.
New commands to change the IO port pin modes are 10-45, 10-46, 10-47 and 10-48.

Mode	Low State	High State	ModeBit1	ModeBit0
0	Hi-Z	Hi-Z	0	0
1	Medium Sink (8mA)	High Drive[2]	0	1
2	Low Sink (2mA)	Resistive 14K-ohm[1]	1	0
3	High Sink (50mA) [3]	High Drive[2]	1	1

Note1 – Boot up default state.
Note2 – Maximum Cumulative Drive for all port pins is 30mA.
Note3 – Maximum Cumulative Sink for all port pins is 70mA.

Certain operating modes automatically change the port pins modes.
I2C: When the user uses the I2C functions the SCL and SDA pins are switched to mode 1 except when receiving where it uses mode 2.

Firmware Commands Differences:
Below are the changed or appended firmware commands. For a complete command list see the USBIODS.pdf and USBIODS7.pdf links below.

Ignored old commands. This command may still be sent but will be ignored.
10-30 Setup port 0 pull up.
10-31 Setup port 1 pull up.
10-32 Setup port 0 sink current.
10-33 Setup port 1 sink current.

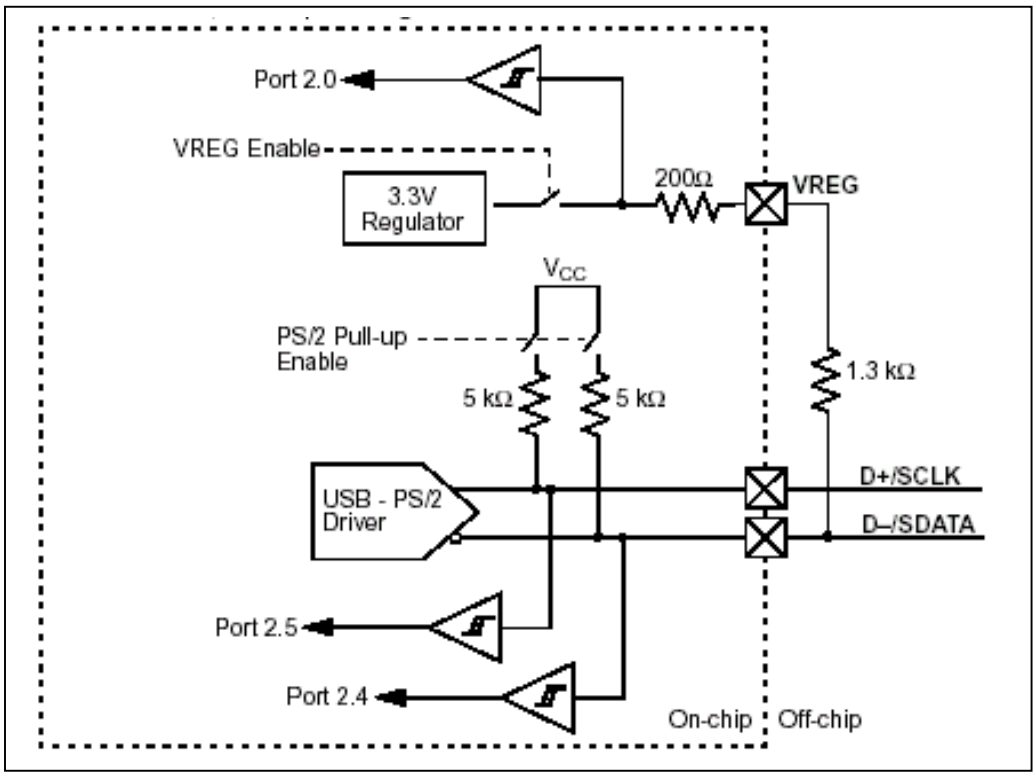
New commands added:
10-43 Set port 0 interrupt level. See CY7C637xx-B.pdf Section 12.0.
10-44 Set port 1 interrupt level. See CY7C637xx-B.pdf Section 12.0.
10-43 and 10-44 are used to set the interrupt edge of event counter command.

10–45 Setup port 0 ModeBit0 mode. See CY7C637xx-B.pdf Section 12.0.
10–46 Setup port 0 ModeBit1 mode. See CY7C637xx-B.pdf Section 12.0.
10–47 Setup port 1 ModeBit0 mode. See CY7C637xx-B.pdf Section 12.0.
10–48 Setup port 1 ModeBit1 mode. See CY7C637xx-B.pdf Section 12.0.

Other Optional Differences:
These differences are optional; the older way will still work.

Internal clock: The new chip has an internal clock. Therefore the external clock is not required any more. Furthermore the clock pin input can now be uses as input. This pin can be read with command 11-0 byte 3 of 7, bit 1 of 7.

Internal 3.3v Regulator: The new chip has a internal 3.3v regulator that is used for the D- pull up. See schematic below. Note the D- pull up is 1.3K instead of 7.5K. When/if you relay out your PCB you should uses this arrangement because it has improved noise immunity then the original layout. The 3.3v regulator is only to be used for the D- pull up, it doesn't have the power to drive anything else.



Related links:
Delcom Website: www.delcom-eng.com
Delcom USB IO Datasheet 802x00: www.delcom-eng.com/downloads/USBIODS.pdf
Delcom USB IO Datasheet 802x70: www.delcom-eng.com/downloads/USBIODS7.pdf

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